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**BI-MONTHLY PROGRESS REPORT NO. 1  
PROJECT NORTHVILLE**

**Period July 15, 1959 to August 30, 1959**

**REPORT OF WORK UNDER  
CONTRACT NO. 635**

**WITH**

**U. S. GOVERNMENT**

50X1

**SUBMITTED BY:**

[Redacted Signature Box]

**Project Engineer**

**APPROVED BY:**

**ORIGINAL SIGNED**

[Redacted Signature Box]

**Manager  
Program 684**

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**ORIGINAL CL BY** 235979  
**DECL** ☒ **REVISION** 2010  
**EXT BYND 6 YRS BY** SAME  
**REASON** 3 d(3)

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**DOCUMENT NO.** \_\_\_\_\_  
**NO CHANGE IN CLASS.** ☐  
☐ **DECLASSIFIED**  
**CLASS. CHANGED TO:** TS S 2010  
**NEXT REVIEW DATE:** \_\_\_\_\_  
**AUTH:** HR 70-2  
**DATE:** 9 DEC 1980 **REVIEWER:** 064540

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Design and develop coincident-current buffer memory packaged within the minimum volume possible. Low cost, standard techniques are to be used where possible. One prototype to be furnished for test and evaluation. Four additional units to be fabricated after approval of prototype.

**II ACCOMPLISHMENTS**

1. Conferences: Conference Report No. 1 held on July 22, 1959 at [redacted] Corporation, Defense Sales Office, Washington, D. C. The purpose of this conference was to discuss packaging and circuit details of buffer memory device. 50X1

Conference Report No. 2 held on August 10, 1959 at [redacted] Pa. The purpose of this conference was to decide on memory capacity as determined by options in Conference Report No. 1. 50X1

2. Reports: None.
3. Expenditures: Information concerning the utilization of funds during the period will be submitted by a separate report to the Contracting Officer.
4. Schedule: The Project Schedule included with this report was based on the effort commencing 1 July 1959. The allotting of funds did not occur until 15 July 1959. There is, therefore, a two-week overall delay. The package design schedule has been extended two weeks but no effect is expected on the end date. The circuit design schedule is still firm, but some slippage could occur. Again there is no expected effect on the end date. The sub-system and unit fabrication have not been started but schedule slippage in this area is expected to be regained once the design effort has been accomplished.

The requirements for the memory have been finalized and the logical design is completed. The major circuit designs have been completed with some testing remaining. All of the basic circuits such as current amplifiers, oscillators, and logic elements will be bench tested before final release for packaging. The magnetic core and transistor evaluation is in process. An overall layout of the memory unit has been completed. This includes the 2560 bit memory, the diode matrix, component boards, interconnecting backboard, and chassis configuration. The memory assembly has been completely detailed and portions are being fabricated to prove out the design. A portion of the diode matrix has been detailed and an experimental assembly will also be fabricated. The component boards, which will contain the circuitry for the logic elements, have been laid out on a preliminary basis. Complete detailing of the component boards is awaiting release of the circuit designs.

**III PROBLEMS**

None.

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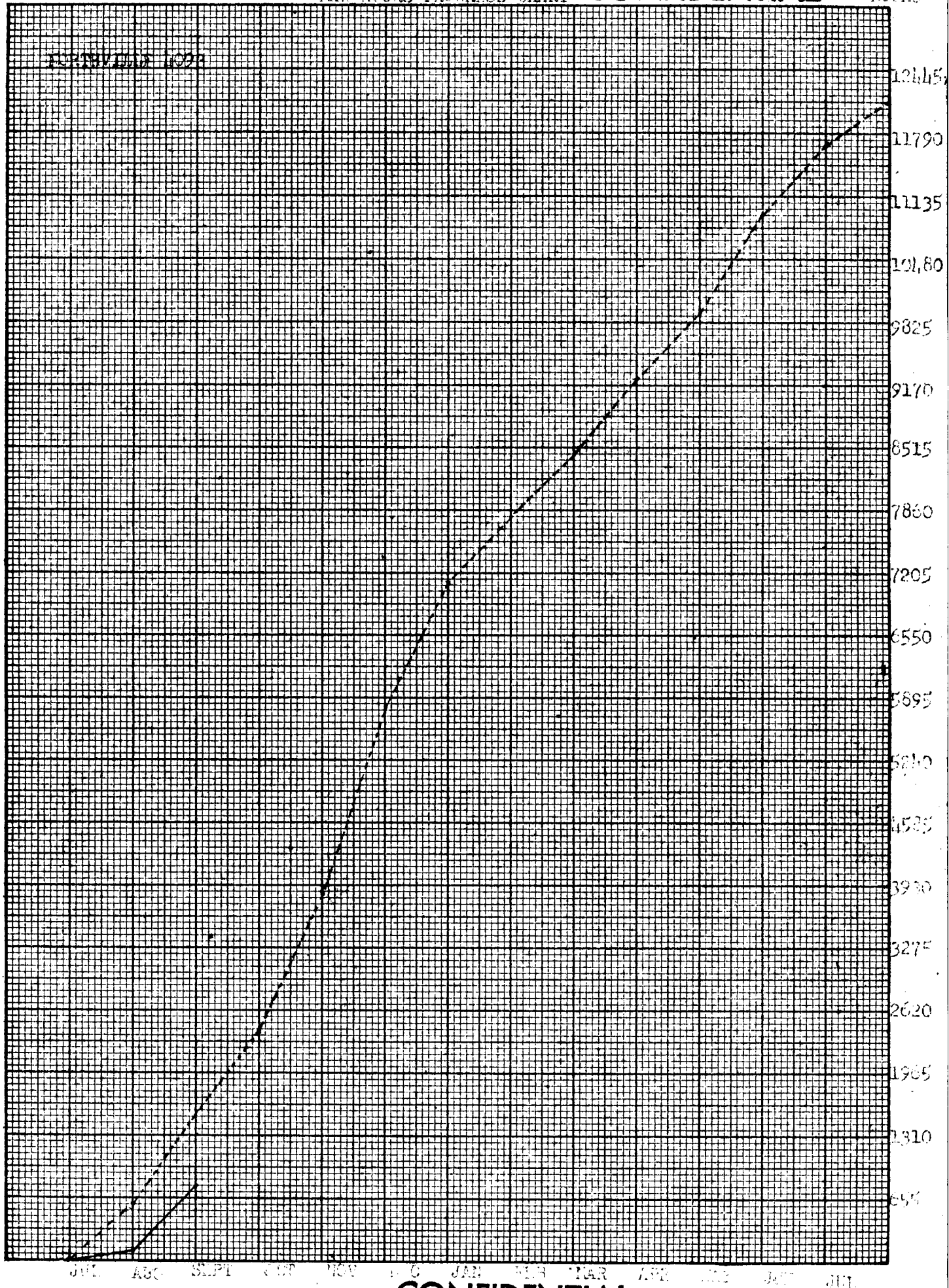
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#### IV FUTURE PLANS

During the next bi-monthly period the effort will be concentrated on those areas that will aid in regaining schedule slippage. Particularly, completion of the circuit design effort will be a major goal. The parts requirement will be detailed early in the period to allow ordering to be accomplished as early as possible. The electrical parts are not expected to present procurement difficulties. As the memory section will be ready for fabrication plans will be made to begin assembly upon receipt of components. The packaging effort will be concentrated on the component board details followed by the details for the interconnecting backboard. After this the controls and battery assembly will be considered.

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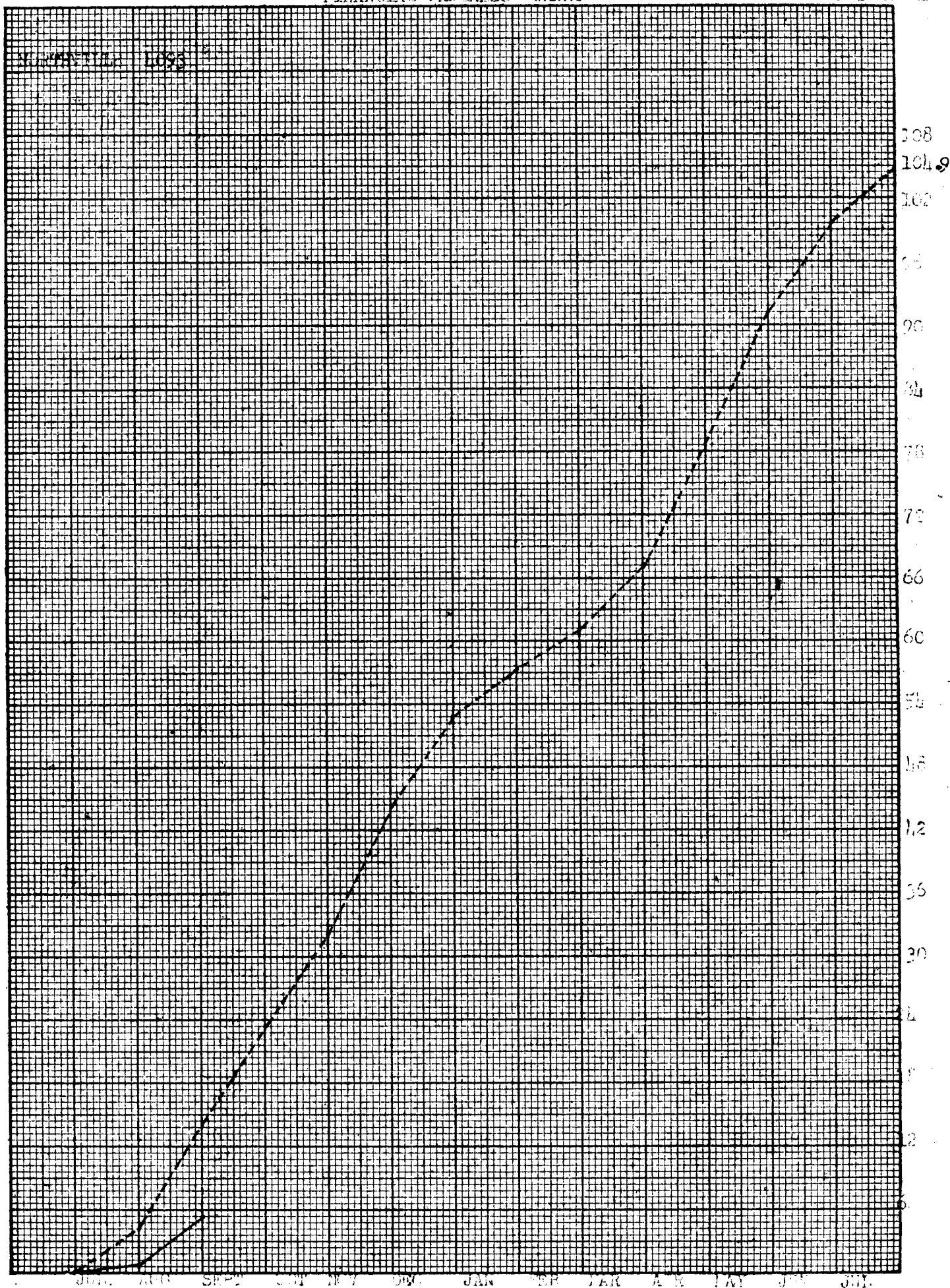
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**SPECIAL PRODUCTS DIVISION  
PROJECT SCHEDULE**

PROJECT ENGR. \_\_\_\_\_  
ADMIN. ENGR. \_\_\_\_\_  
REVISION \_\_\_\_\_ 7-22-59

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